

A cross-sectional view of a semiconductor device. A substrate 102 is shown at the bottom, with a ground symbol connected to it via a line 124. A layer 101 is on top of the substrate. A gate stack is formed on the substrate, consisting of a gate dielectric 105 and a gate electrode 106. The gate stack is divided into three regions labeled S, G, and D. Source and drain regions 107 are formed on the substrate, with a p+ region on the left and a p- region on the right. A p+ region is also shown on the left side of the substrate. A layer 121 is on top of the substrate, and a layer 122 is on top of the gate stack. A PSG layer is on top of the substrate on the right side. A line 101 points to the substrate, and a line 102 points to the gate stack.

Fig. 4